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U.S. PATENT DOCUMENTS

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EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
JRW		Nagata, M., et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits," IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, (Mar. 2001).
JRW		Nagata, M., et al, "Quantitative Characterization of Substrate Noise for Physical Design Guides in Digital Circuits," IEEE 2000 Custom Integrated Circuits Conference, Orlando, Florida, May 21-24, 2000.
JRW		Table of Contents for the Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, Orlando, Florida, May 21-24, 2000.

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JRW	04/22/04

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